What is claimed is:

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1. An electrical semiconductor device comprising:
a substrate of relatively high resistivity material of one conductivity type having opposing first and second surfaces, the first surface being etched;
a layer of relatively low resistivity material of the one conductivity type and having one surface substantially contiguous to the first surface of the substrate; and
an epitaxial region of relatively low resistivity material of a conductivity type opposite to the one conductivity type and having one surface substantially contiguous to the second surface of the substrate.

2. The device of claim 1 wherein the layer is diffused into the first surface of the substrate.

3. The device of claim 1 wherein the layer is epitaxially grown onto the first surface of the substrate.

4. The device of claim 1 wherein the epitaxial region includes a stress-relieving dopant.

5. The device of claim 4 wherein the stress-relieving dopant is germanium.

6. An electrical semiconductor device comprising:
an epitaxial layer of relatively high resistivity material of one conductivity type and having opposing first and second surfaces;
a substrate of relatively low resistivity material of a conductivity type opposite to the one conductivity type and having a surface substantially contiguous to the first surface of the epitaxial layer; and
a dopant region of relatively low resistivity material of the one conductivity type having a surface substantially contiguous to the second surface of the epitaxial layer.

7. The device of claim 6 wherein the second surface is etched, and the dopant region is diffused into the second surface of the epitaxial layer.

8. The device of claim 6 wherein the second surface is etched, and the dopant region is epitaxially grown onto the second surface of the epitaxial layer.

9. The device of claim 6 wherein a silicon oxide mask is applied to the first surface of the substrate and the layer is diffused through the silicon oxide mask and into the second surface of the substrate.

10. The device of claim 6 wherein the epitaxial region includes a stress-relieving dopant.

11. The device of claim 10 wherein the stress-relieving dopant is germanium.

12. An electrical semiconductor device comprising:

an epitaxial layer of relatively high resistivity material of one conductivity type and having opposing first and second surfaces, the epitaxial layer further having a dopant material permeated throughout the layer;

a substrate of relatively low resistivity material of a conductivity type opposite to the one conductivity type and having a surface substantially contiguous to the first surface of the epitaxial layer; and

a region of relatively low resistivity material of the one conductivity type having a surface substantially contiguous to the second surface of the epitaxial layer.

13. The device of claim 12 wherein the dopant is a stress-relieving dopant.

14. The device of claim 13 wherein the stress-relieving dopant is germanium.

15. The device of claim 12 wherein a silicon oxide mask is applied to the second surface of the epitaxial layer and the region is diffused through the silicon oxide mask and into the second surface of the epitaxial layer.

16. A method for fabricating an electrical semiconductor device comprising:

selecting a substrate of relatively low conductive material of one conductivity type, the substrate having opposing first and second surfaces;
etching the first surface of the substrate;
diffusing a region of high conductivity material of the one conductivity type into the first surface of the substrate; and
growing an epitaxial layer of high conductivity material onto the second surface of the substrate, the epitaxial layer having a conductivity type opposite to the one conductivity type.

17. A method for fabricating an electrical semiconductor device comprising:
preparing a substrate of relatively low conductivity material of one conductivity type, the substrate having opposing first and second surfaces;
etching the first surface of the substrate;
growing a first epitaxial layer of high conductivity material of the one conductivity type onto the first surface of the substrate; and
growing a second epitaxial layer of high conductivity material onto the second surface of the substrate, the second epitaxial layer having a conductivity type opposite to the one conductivity type.

18. A method for fabricating an electrical semiconductor device comprising:
selecting a substrate of relatively high conductivity material of one conductivity type, the substrate having a first surface;
growing an epitaxial layer onto the first surface of the substrate, the epitaxial layer having opposing first and second surfaces, with the first epitaxial surface being substantially contiguous to the first surface of the substrate, and being of a low conductivity material of a conductivity type opposite to the one conductivity type;
introducing a dopant material to the epitaxial layer;
applying a silicon oxide layer to the second epitaxial surface;
creating a silicon oxide mask by etching portions of the silicon oxide layer to expose portions of the second epitaxial surface; and

diffusing a high conductivity layer through the mask and into the second epitaxial layer, the diffused layer being of a conductivity type opposite to the one conductivity type

19. The device of claim 18 wherein the dopant material is a stress-relieving dopant material.

20. The device of claim 18 wherein the stress-relieving dopant material is germanium.

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21. An electrical semiconductor device comprising:

a first layer of relatively high resistivity material of one conductivity type having opposing first and second surfaces;

a second layer of relatively low resistivity material of a conductivity type opposite to the one conductivity type and having one surface substantially contiguous to the first surface of the substrate;

a region of relatively low resistivity material of the one conductivity type and having one surface substantially contiguous to the second surface of the substrate; and

a substantially centrally located well formed in the first layer such that the distance between the region and the second layer is reduced at the location of the well.

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